National Semiconductor

February 1995

LM122/LM322/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The **trigger** input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V—even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the $\mathbf{V_{ADJ}}$ pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A **boost** terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3 μs to multi-hour timing range with excellent repeatability.

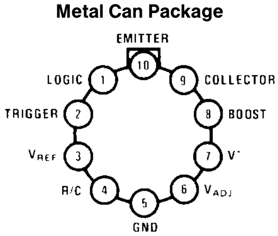
The LM122 operates over a temperature range of −55°C to +125°C. An electrically identical LM322 is specified from 0°C to +70°C. The LM3905 is identical to the LM122 series except that the **boost** and $\mathbf{V_{ADJ}}$ pin options are not available, limiting minimum timing period to 1 ms.

Features

- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to ±40V
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

Connection Diagrams

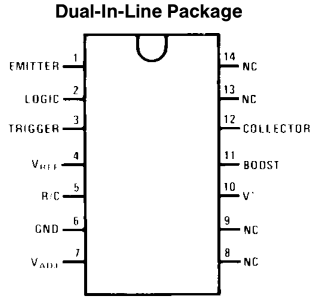
Metal Can Package



TL/H/7768–6

Top View
Order Number LM122H
See NS Package Number H10C

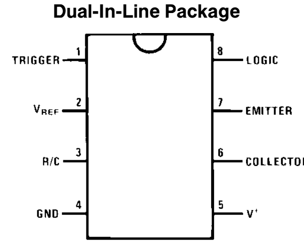
Dual-In-Line Package



TL/H/7768–7

Top View
Order Number LM322N
See NS Package Number N14A

Dual-In-Line Package



TL/H/7768–8

Top View
Order Number LM3905N
See NS Package Number N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	500 mW
V^+ Voltage	40V
Collector Output Voltage	40V
V_{REF} Current	5 mA
Trigger Voltage	±40V
V_{ADJ} Voltage (Forced)	5V
Logic Reverse Voltage	5.5V
Output Short Circuit Duration (Note 1)	
Lead Temperature (Soldering, 10 sec.)	260°C
Operating Temperature Range	
LM122	$-55°C \le T_A \le +125°C$
LM322	$0°C \le T_A \le +70°C$
LM3905	$0°C \le T_A \le +70°C$

Electrical Characteristics (Note 2)

Parameter	Conditions	LM122			LM322			LM3905			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Timing Ratio	$T_A = 25°C$, $4.5V \le V^+ \le 40V$ Boost Tied to V^+, (Note 3)	0.626 0.620	0.632 0.632	0.638 0.644	0.620 0.620	0.632 0.632	0.644 0.644	0.620	0.632	0.644	
Comparator Input Current	$T_A = 25°C$, $4.5V \le V^+ \le 40V$ Boost Tied to V^+		0.3 30	1.0 100		0.3 30	1.5 100		0.5	1.5	nA nA
Trigger Voltage	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2	V
Trigger Current	$T_A = 25°C$, $V_{TRIG} = 2V$		25			25			25		μA
Supply Current	$T_A \ge 25°C$, $4.5V \le V^+ \le 40V$		2.5	4		2.5	4.5		2.5	4.5	mA
Timing Ratio	$4.5V \le V^+ \le 40V$ Boost Tied to V^+	0.62 0.62		0.644 0.644	0.61 0.61		0.654 0.654	0.61		0.654	
Comparator Input Current	$4.5V \le V^+ \le 40V$ Boost Tied to V^+, (Note 4)	−5		5 100	−2		2 150	−2.5		2.5	nA nA
Trigger Voltage	$4.5V \le V^+ \le 40V$	0.8		2.5	0.8		2.5	0.8		2.5	V
Trigger Current	$V_{TRIG} = 2.5V$			200			200			200	μA
Output Leakage Current	$V_{CE} = 40V$			1			5			5	μA
Capacitor Saturation Voltage	$R_t \ge 1\ M\Omega$ $R_t = 10\ k\Omega$		2.5 25			2.5 25			2.5 25		mV mV
Reset Resistance			150			150			150		Ω
Reference Voltage	$T_A = 25°C$	3	3.15	3.3	3	3.15	3.3	3	3.15	3.3	V
Reference Regulation	$0 \le I_{OUT} \le 3\ mA$ $4.5V \le V^+ \le 40V$		20 6	50 25		20 6	50 25		20 6	50 25	mV mV
Collector Saturation Voltage	$I_L = 8\ mA$ $I_L = 50\ mA$		0.25 0.7	0.4 1.4		0.25 0.7	0.4 1.4		0.25 0.7	0.4 1.4	V V
Emitter Saturation Voltage	$T_A = 25°C$, $I_L = 3\ mA$ $T_A = 25°C$, $I_L = 50\ mA$		1.8 2.1	2.2 3		1.8 2.1	2.2 3		1.8 2.1	2.2 3	V V
Average Temperature Coefficient of Timing Ratio			0.003			0.003			0.003		%/°C
Minimum Trigger Width	$V_{TRIG} = 3V$		0.25			0.25			0.25		μs

Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = 120/V_{CE}$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

Note 2: These specifications apply for $T_{AMIN} \le T_A \le T_{AMAX}$ unless otherwise noted.

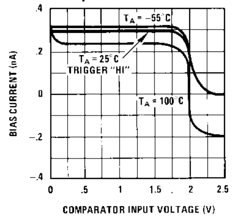
Note 3: Output pulse width can be calculated from the following equation: $t = (R_t)(C_t)[1 - 2(0.632 - r) - V_C/V_{REF})$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_t)(C_t)$ for all but the most critical applications.

Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typcial curves.

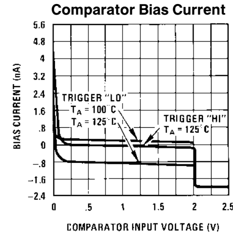
Note 5: Refer to RETS122X drawing of military LM122H version for specifications.

Typical Performance Characteristics

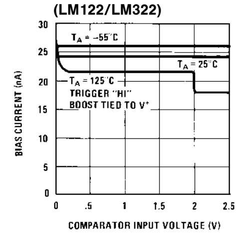
Comparator Bias Current



Comparator Bias Current

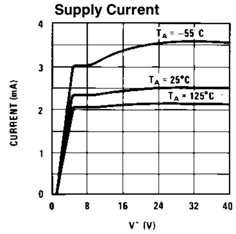


Comparator Bias Current (LM122/LM322)

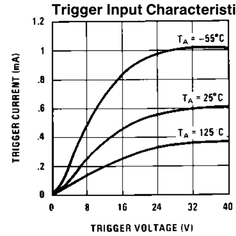


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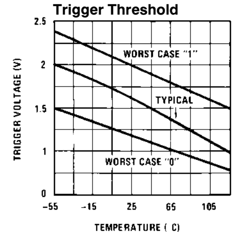
Supply Current



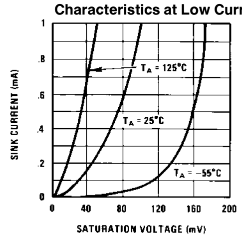
Trigger Input Characteristics



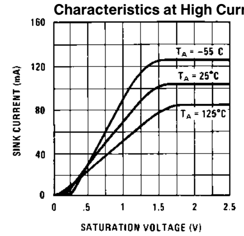
Trigger Threshold



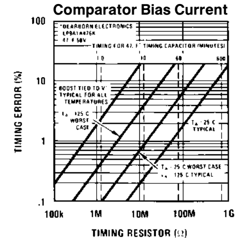
Output Transistor Saturation Characteristics at Low Currents



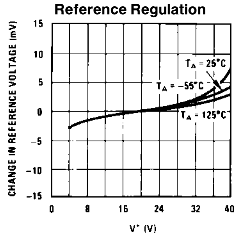
Collector Output Saturation Characteristics at High Current



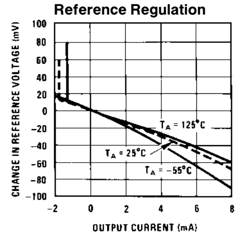
Timing Error Due to Comparator Bias Current



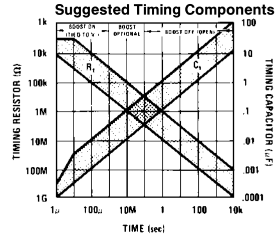
Reference Regulation



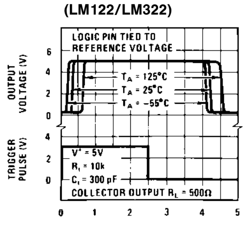
Reference Regulation



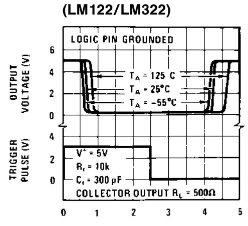
Suggested Timing Components



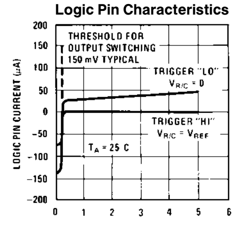
Short Output Pulse (LM122/LM322)



Short Output Pulse (LM122/LM322)

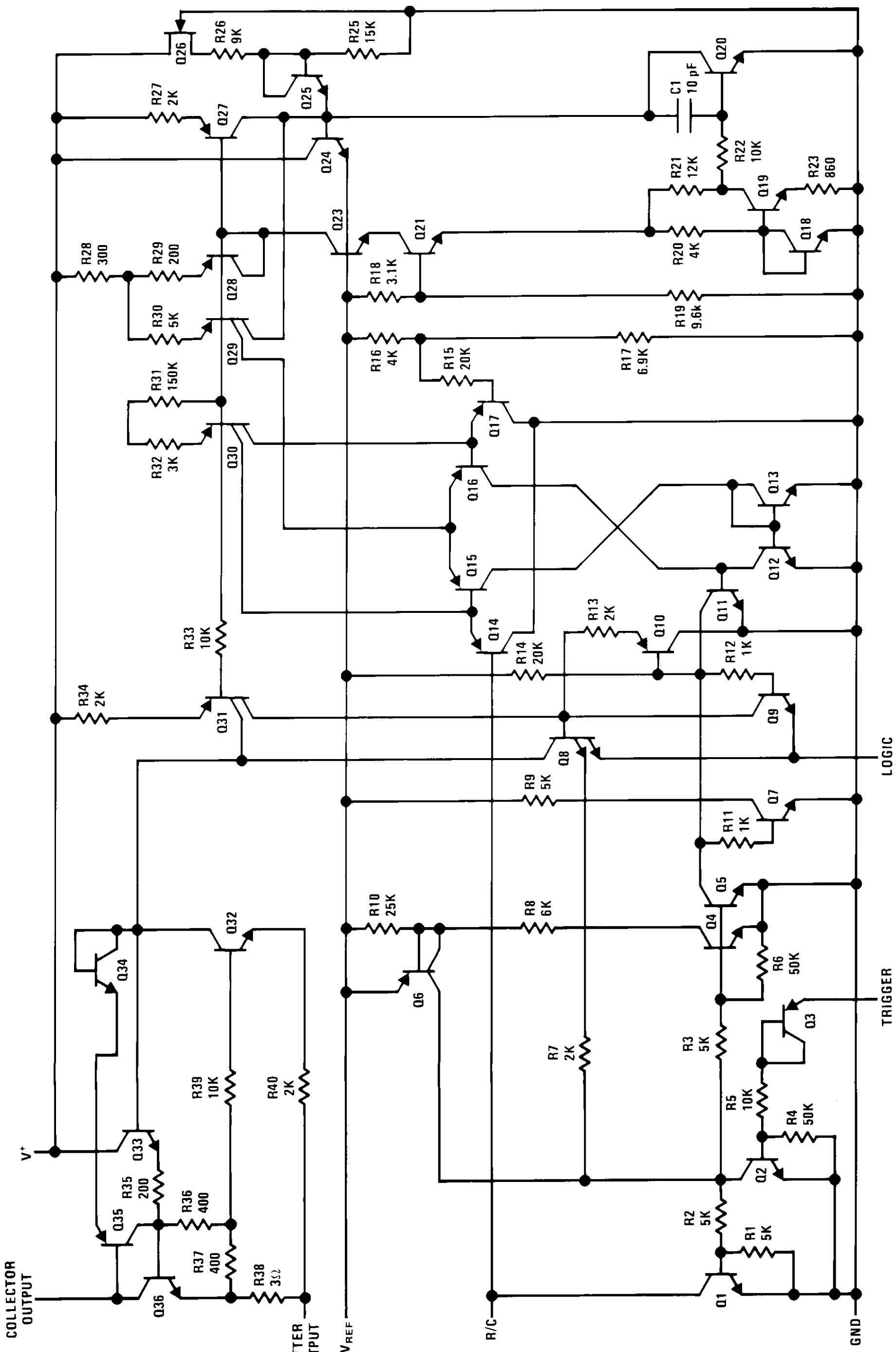


Logic Pin Characteristics



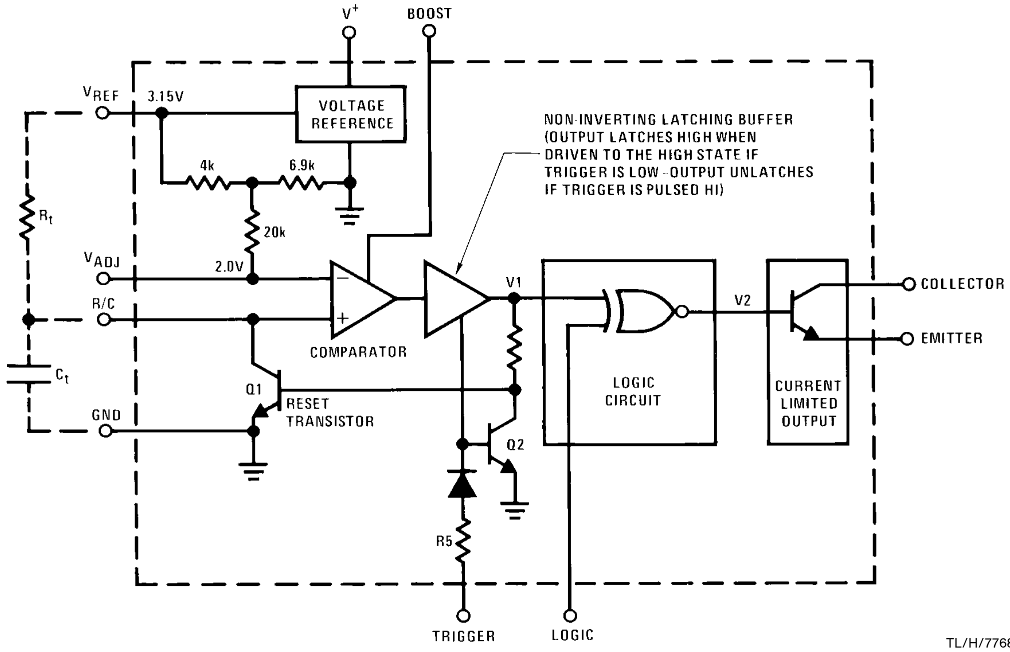
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Schematic Diagram



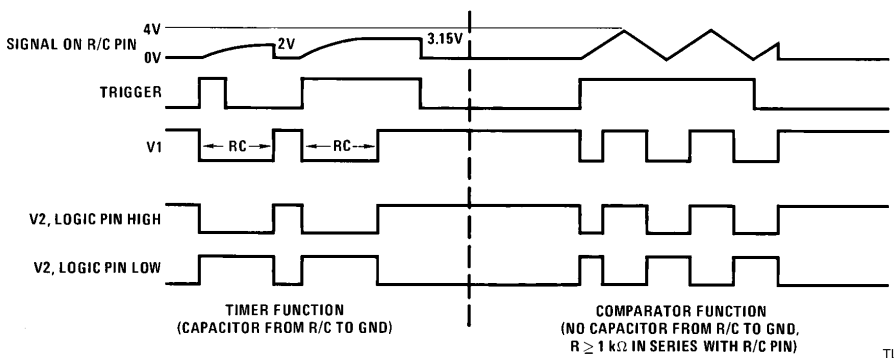
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Functional Diagram



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Timing Diagram



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Pin Function Description

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on **V+** is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the **V+** terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The $\mathbf{V_{REF}}$ pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to $\mathbf{V_{REF}}$, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature con-

Pin Function Description (Continued)

trollers. Typical temperature drift of the reference is less than 0.01%/°C.

The **trigger** terminal is used to start a timing cycle (see functional diagram). Initially, Q1 is saturated, C_t is discharged and the latching buffer output (V1) is latched high. A trigger pulse unlatches the buffer, V1 goes low and turns Q1 off. The timing capacitor C_t connected from R/C to GND will begin to charge. When the voltage at the R/C terminal reaches the 2.0V threshold of the comparator, the comparator toggles, latching the buffer output (V1) in the high state. This turns on Q1, discharges the capacitor C_t and the cycle is ready to begin again.

If the **trigger** is held high as the timing period ends, the comparator will toggle and V1 will go high exactly as before. However, V1 will not be latched and the capacitor will not discharge until the trigger again goes low. When the trigger goes low, V1 remains high but is now latched.

Trigger threshold is typically 1.6V at 25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the **trigger** source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region. The **trigger** can be driven from supplies as high as ±40V, even when device supply voltage is only 5V.

The **R/C** pin is tied to the non-inverting side of the comparator and to the collector of Q1. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). Q1 turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the **R/C** pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Current from the **R/C** pin is typically 300 pA when the voltage is negative with respect to the $\mathbf{V_{ADJ}}$ terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is typically 30 nA. Gain of the comparator is very high, 200,000 or more, depending on the state of the logic reverse pin and the connection of the output transistor.

The **ground** pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the $\mathbf{V^+}$ terminal. Level shifting may be necessary for the input **trigger** if the **trigger** voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the **ground** terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the **ground** pin of the LM122 was tied to a negative supply.

The terminal labled $\mathbf{V_{ADJ}}$ is tied to one side of the comparator and to a voltage divider between $\mathbf{V_{REF}}$ and **ground**. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to $\mathbf{V_{ADJ}}$. This resistor is a pinched type with a typical variation in nominal value of −50%, +100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between $\mathbf{V_{REF}}$ and **ground**) connected to $\mathbf{V_{ADJ}}$ should have a source resistance as low as possible. For small changes in $\mathbf{V_{ADJ}}$, up to several kΩ is all right, but for large variations, 250Ω or less should be maintained. This can be accomplished with a 1k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on $\mathbf{V_{ADJ}}$ from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The $\mathbf{V_{ADJ}}$ pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high, when the $\mathbf{V_{ADJ}}$ pin is grounded. In this case, the output changes state, but the capacitor does not discharge.

If the trigger drops while $\mathbf{V_{ADJ}}$ is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when $\mathbf{V_{ADJ}}$ is released, the output may or may not change state, depending on the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output. This pin is not available on the LM2905/LM3905.

In noisy environments or in comparator-type applications, a bypass capacitor on the $\mathbf{V_{ADJ}}$ terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The **emitter** and the **collector** outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the **emitter** is tied to the **ground** pin and the signal is taken from the **collector**, or the **collector** is tied to $\mathbf{V^+}$ and the signal is taken from the **emitter**. Variations on these basic connections are possible. The **collector** can be tied to any positive voltage up to 40V when the signal is taken from the **emitter**. However, the **emitter** will not be pulled higher than the supply voltage on the $\mathbf{V^+}$ pin. Connecting the **collector** to a voltage less than the $\mathbf{V^+}$ voltage is allowed. The **emitter** should not be connected to a low impedance load other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with **collector-emitter** voltages up to 40V. The power x time product, however, must not exceed 15 watt-seconds for power levels above the maximum rating of the package. A short to 30V,

Pin Function Description (Continued)

for instance, cannot be held for more than 4 seconds. These levels are based on 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A **boost** pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current.

For timing periods less than 1 ms, where low input current is not needed, comparator operating current can be increased several orders of magnitude. Shorting the boost terminal to **V+** increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5 μA. This pin is not available on the LM3905.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used. The 800 ns error is relatively insensitive to temperature, so temperature coefficient of pulse width is still good.

The **Logic** pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the **logic** pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the **logic** pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the **logic** pin is typically 100 mV with 150 μA flowing out of the terminal. If an active drive to the **logic** pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 25 mV at 200 μA is required. Minimum and maximum voltages that may appear on the **logic** pin are 0 and +5.0, respectively.

Typical Applications

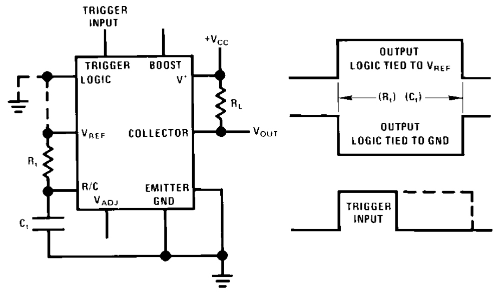
Basic Timers

Figure 1 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch along side *Figure 1*. Note that the trigger pulse may be either shorter or longer than the output pulse width.

Figure 2 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

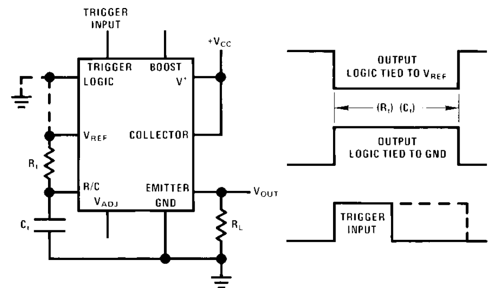
Simulating a Thermal Delay Relay

Figure 3 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 4* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.



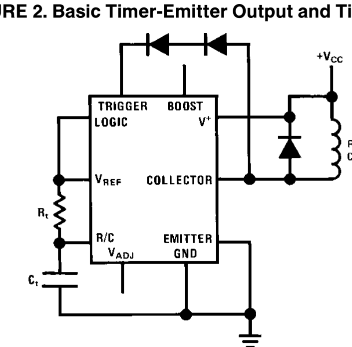
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FIGURE 1. Basic Timer-Collector Output and Timing Chart



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FIGURE 2. Basic Timer-Emitter Output and Timing Chart



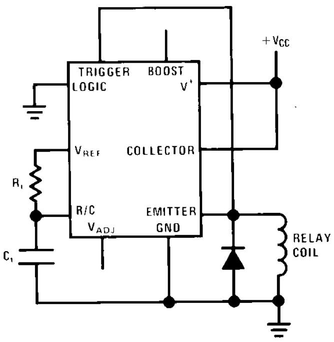
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FIGURE 3. Time Out on Power Up (Relay Energized R_t C_t Seconds after V_{CC} is Applied)

+5V Supply Driving 28V Relay

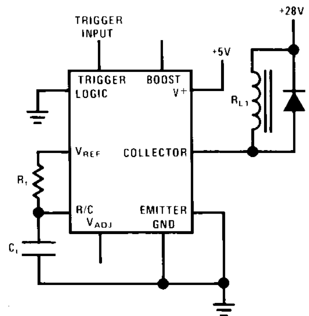
Figure 5 shows the timer interfacing 5V logic to a high voltage relay. Although the V^+ terminal could be tied to the +28V supply, this may be an unnecessary waste of power in the IC or require extra wiring if the LM122 is on a logic card. In either case, the threshold for the trigger is 1.6V.

Typical Applications (Continued)



TL/H/7768–14

FIGURE 4. Time Out on Power Up (Relay Energized *Until* R_t C_t Seconds After V_{CC} is Applied)

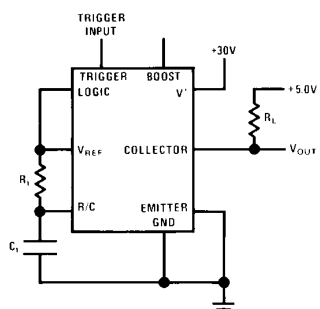


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FIGURE 5. 5V Logic Supply Driving 28V Relay

30V Supply Interfacing with 5V Logic

Figure 6 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL. If the logic is sensitive to rise/fall time of the trailing edge of the output pulse, the trigger pin should be low at that time.

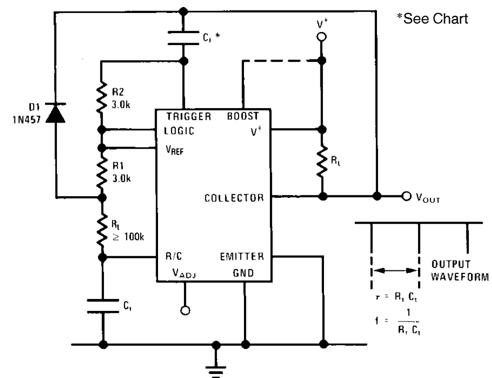


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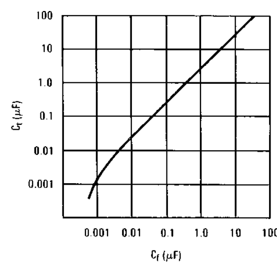
FIGURE 6. 30V Supply Interfacing with 5V Logic

Astable Operation

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in *Figure 7*. Operating frequency is $1/(R_t + R_1)(C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t \geq$ 500k.



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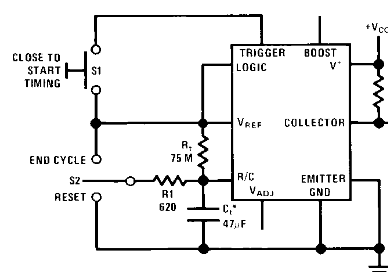


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FIGURE 7. Oscillator

One Hour Timer with Reset and Manual Cycle End

Figure 8 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released.



*Dearborn Electronics LP9A1A476K Polycarbonate

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FIGURE 8. One Hour Timer with Reset and Manual Cycle End

Typical Applications (Continued)

The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

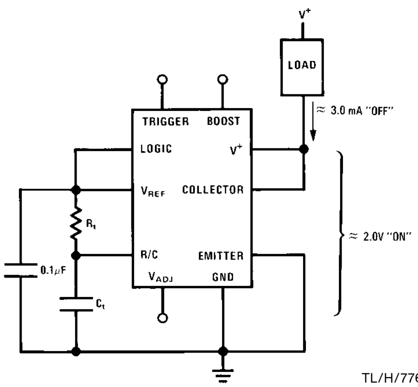
Two Terminal Time Delay Switch

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In *Figure 9*, the timer is used to drive a relay "on" $R_t \bullet C_t$ seconds after application of power. "Off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

Zero Power Dissipation Between Timing Intervals

In some applications it is desirable to reduce supply current drain to zero between timing cycles. In *Figure 10* this is accomplished by using an external PNP as a latch to drive the V^+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents the step on the V^+ pin from coupling back into the trigger pin. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.



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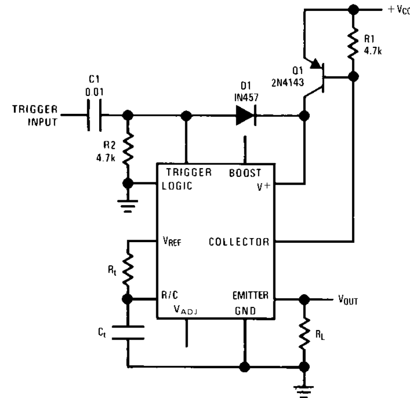
FIGURE 9. 2-Terminal Time Delay Switch

Frequency to Voltage Converter

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 11*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

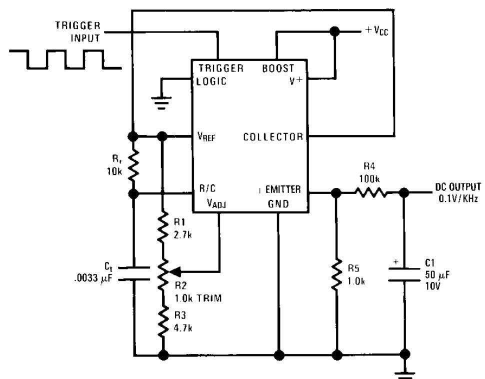
Pulse Width Detector

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made *(Figure 12)*.



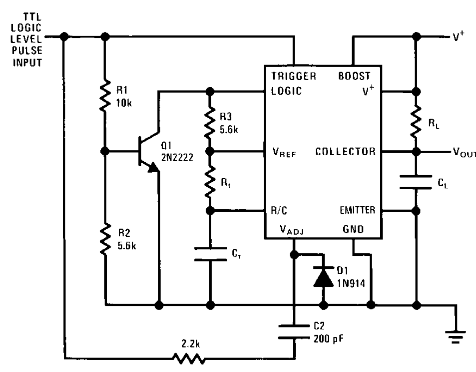
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FIGURE 10. Zero Power Dissipation Between Timing Intervals



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FIGURE 11. Frequency to Voltage Converter. (Tachometer) Output Independent of Supply Voltage.



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$^*V_{OUT} = 0$ for $W\ R_1\ C_1$

Pulse Out $= W - R_1\ C_1$ for $W\ R_1\ C_1$

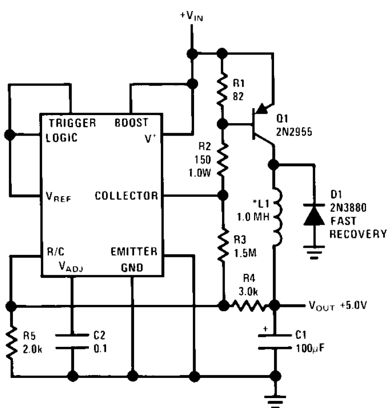
FIGURE 12. Pulse Width Detector

Typical Applications (Continued)

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short (<RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to propagation delays during switching.

5V Switching Regulator

Figure 13 is an application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP transistor switch. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.



*No. 22 Wire Wound on Molybdenum Permalloy Core TL/H/7768–24

FIGURE 13. 5V Switching Regulator with 1 Amp Output and 5.5V Minimum Input

Application Hints

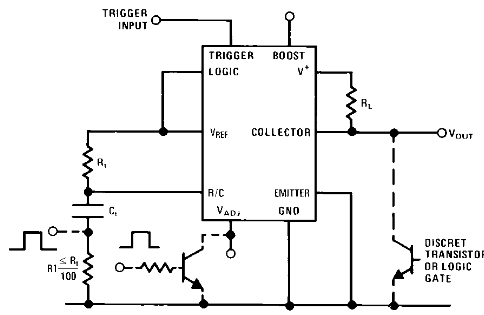
Aborting a Timing Cycle

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may also be ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.



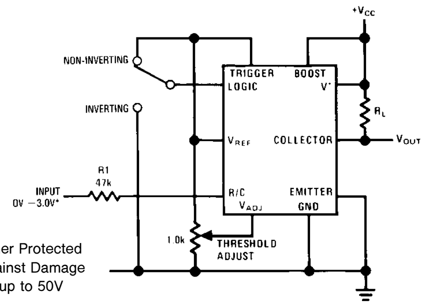
TL/H/7768–25

FIGURE 14. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 15*. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply with internal reference should make this comparator very useful.



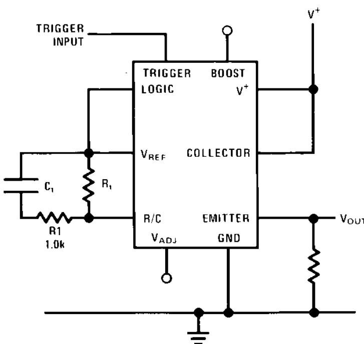
*Timer Protected Against Damage for up to 50V

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FIGURE 15. Comparator with 0V to 3V Threshold

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will normally start a timing cycle (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 16*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

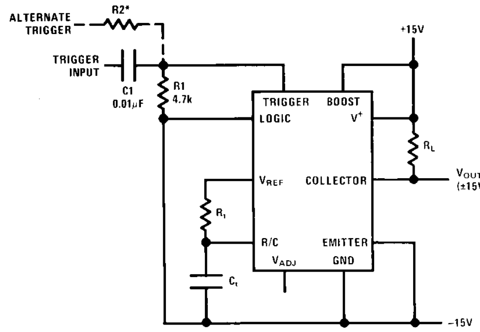


TL/H/7768–27

FIGURE 16. Eliminating Initial Timing Cycle

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in *Figure 17*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



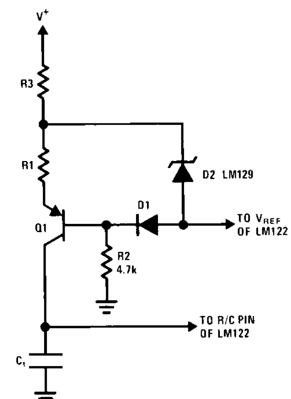
TL/H/7768–28

*Select for Proper Level Shift
Emitter Terminal or Emitter Load must be Tied to GND Pin of Timer

FIGURE 17. Operating Off Dual Supplies

Linearizing the Charging Sweep

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in *Figure 18*.



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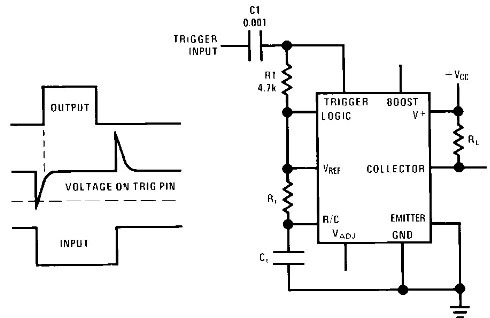
FIGURE 18. Temperature Compensated Linear Charging Sweep

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability is not critical. With D1, D2, R2 and R3 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

Triggering with Negative Edge

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 19*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately (0.5 to 1.5) (R1 • C1) depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

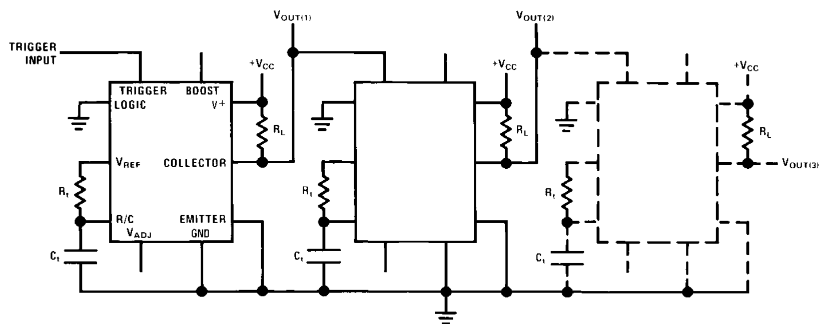


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FIGURE 19. Timer Triggered by Negative Edge of Input Pulse

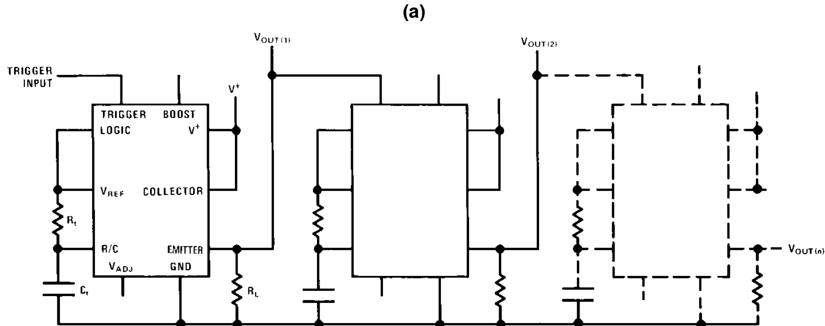
Chain of Timers

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 20A* and *20B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of the timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

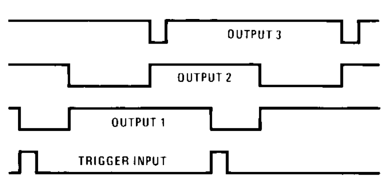


TL/H/7768–31

(a)



TL/H/7768–32

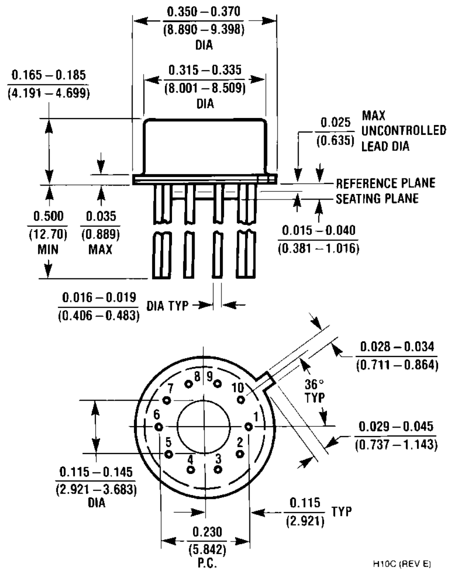


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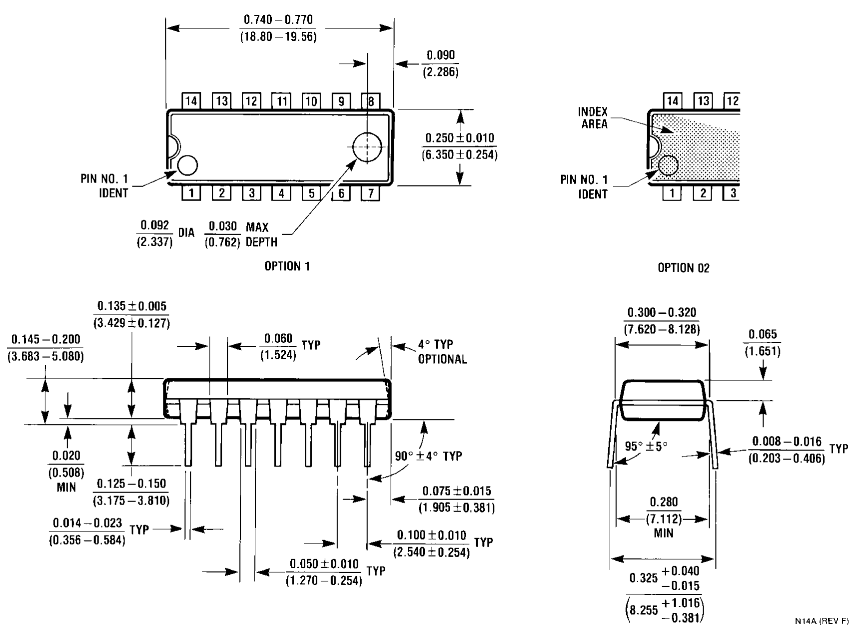
(b)

FIGURE 20. Chain of Timers

Physical Dimensions inches (millimeters)

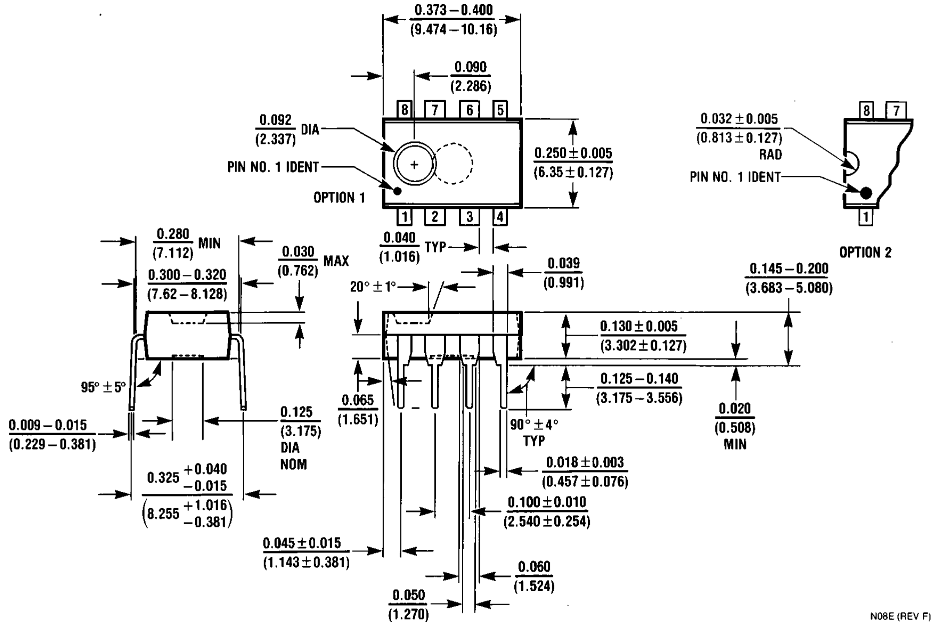


Metal Can Package (H)
Order Number LM122H
NS Package Number H10C



Dual-In-Line Package (N)
Order Number LM322N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line Package (N)
Order Number LM3905N
NS Package Number N08E

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